The opinion in support of the decision being entered today was <u>not</u> written for publication and is <u>not</u> binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte TAKEO YASUHO, MASAO IWATA, RYOICHI KATSURAGAWA, HAYAMI MATSUNAGA, YOSHIKAZU SUEHIRO, and YASUHIKO YOKOTA

Appeal No. 1999-1454
Application No. 08/596,343¹

HEARD: March 21, 2001

Before JERRY SMITH, RUGGIERO, and LEVY, <u>Administrative Patent</u> <u>Judges</u>.

LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-15, which are all of the claims pending in this application.

 $^{^{\}rm 1}$ Application filed under 35 U.S.C. § 371 based upon PCT/JP95/01326 filed on July 3, 1995, claiming foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application No. 6/152177, filed July 4, 1994.

Appeal No. 1999-1454
Application No. 08/596,343

BACKGROUND

The appellants' invention relates to an integrated circuit. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

- 1. An integrated circuit device comprising:
- a metal board having a CPU power converter which includes one of a DC/DC converter and an AC/DC converter for converting a supply voltage from a motherboard into a driving voltage for driving a CPU chip;
- a multi-layer circuit wiring board having a plurality of pin terminals fitted therein and electrically connected to said CPU power converter on the metal board;
- a CPU chip electrically connected to said multi-layer circuit wiring board between said metal board and said multi-layer circuit wiring board;
- a control section electrically connected to said multi-layer circuit wiring board on a surface opposite to the CPU chip provided on said multi-layer circuit wiring board; and
- a connector electrically connected to said multi-layer circuit wiring board.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Lin 5,222,014 Jun. 22, 1993 Karabatsos et al 5,469,330 Nov. 21,1995

(Karabatsos) (effectively filed Feb. 14, 1994)

Admitted prior art relied upon by the examiner²

Hosen 2264389 A (GB) Aug. 25, 1993

Claims 1-9 and 11-14 stand rejected under 35 U.S.C. § 103 as being unpatentable over the admitted prior art in view of Hosen taken together with Lin.

Claims 10 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over the admitted prior art, Hosen and Lin, and further in view of Karabatsos.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 15, mailed July 20, 1998) for the examiner's complete reasoning in support of the rejections, and to the appellants' brief (Paper No. 14, filed March 27, 1998) and reply brief (Paper No. 17, filed September 23, 1998) for the appellants'

 $^{^2}$ The examiner is not specific as to the specific location of the admitted prior art in the specification. We consider the admitted prior art to be found on page 1, line 8 through page 2, line 4 of the specification.

arguments thereagainst. Only those arguments actually made by the appellants have been considered in this decision.

Arguments which the appellants could have made but chose not to make in the briefs have not been considered. See 37 CFR § 1.192(a).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary

skill in the art the invention set forth in claims 1-15.

Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPO2d 1596, 1598 (Fed. Cir. 1988). so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPO2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221

USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re

Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re

Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We consider first the rejection of claims 1-9 and 11-14 under 35 U.S.C. § 103 based on the teachings of the admitted prior art taken together with Hosen and Lin. We begin with claim 1. The examiner's position (answer, pages 3-4) is that the prior art (specification, page 1) discloses a conventional integrated circuit device wherein the component parts such as the power supply, CPU chip, controllers and connector are all mounted on a single, one-sided or two-sided multi-layer

circuit wiring board. The admitted prior art also refers (<u>id.</u>) to heat radiating plates and a cooling fan.

The examiner asserts (answer, page 3) that Hosen teaches (Figure 3) a related prior art device which includes element 2 requiring high thermal dissipation as well as element 3 requiring less thermal dissipation. Hosen discloses (Figure 2) that the prior art of Figure 3 may be improved by using a two-level approach wherein power chip element 2 requiring high thermal dissipation are placed on a lower metal plate structure 1, and control circuit element 3 requiring less thermal dissipation are placed upon an upper substrate 8.

According to the examiner, (answer, page 4)

It would have been obvious . . . to dispose the elements described by appellant [sic] as conventional in the manner taught by Hosen (i.e. with the elements requiring high thermal dissipation, e.g. power supply and CPU, on the lower metal plate with the remaining elements on an upper substrate) because Hosen teaches that such an arrangement is an improvement over the prior art single-layer approach as it results in a smaller package without a decrease in thermal dissipation.

The examiner notes (<u>id.</u>) that Hosen does not specifically disclose that the upper substrate 8 is a multi-layer circuit wiring board. To overcome this deficiency in Hosen, the

examiner relies upon Lin for a teaching of using a multi-layer circuit wiring board "to electrically connect vertically disposed elements."

Appellants assert (brief, page 7) that the power chip 2 of Hosen does not include a CPU power converter, and that Hosen does not disclose or suggest that the metal board, rather than the multi-layer circuit wiring board has the CPU power converter. Appellants further assert (reply brief, page 1) that "Hosen does not provide any teaching or motivation to move the CPU power converter from its location in the appellants' admitted prior art to its location as recited in present claim 1."

We find that even though the admitted prior art refers to the use of heat radiating plates and a cooling fan, we find no suggestion in the admitted prior art recognizing any problem with having all of the components in a single multi-layer circuit wiring board. We additionally find that Hosen (page 1) is directed to "a structure of a power semiconductor device used for a power transistor module which may be applied to an inverter device." Hosen discloses (pages 1 and 2) that in the

prior art (Figure 3), both the power transistor chip 2, along with the control circuit 3 are mounted on metal insulating plate 1. However, since conductive patterns 1c of metal insulating plate 1 are used as a main circuit wiring connection, it is necessary that a path width of conductive pattern 1c be enlarged so as to obtain a desired electrical capacitance. Hosen discloses (id.) that "the path width must become larger as the electrical capacitance is increased." This (page 2) leads to the desired area of the metal insulating substrate to be increased, "leading to higher cost." Hosen discloses (id.) that the object of the invention is to "provide a power semiconductor device which has a small area substrate and can sufficiently apply a large electrical capacitance." In Figure 2, Hosen discloses (page 5) a two stage stacking structure, leaving the high heat radiation power chips 2 on the insulating metal layer 1, and placing the control circuit 3, which have (page 6) "a calorific value extremely smaller than the power chips 2," on substrate 8 which is above metal insulating layer 1. Hosen further discloses that the metal control circuit substrate 8 is

"formed in the same manner as the [metal insulating] substrate

1." Through the use of the aforementioned structure, Hosen

discloses (id.) that

The formation of a wide internal wiring pattern on a copper foil of the substrate is not needed, and the cross-sectional area of the terminal plate can be freely selected in accordance with the electrical capacitance of power chips. Therefore, a power semiconductor device having a large electrical capacitance can be constructed on a metal insulating structure having a small area.

We thus find that the admitted prior art did not recognize any problems associated with having all of the components on a single multi-layer circuit wiring board. We further find that Hosen is not directed to a CPU chip or CPU power converter, and uses a two-stage stacking structure to avoid the use of a wide internal wiring pattern in order to produce a power semiconductor having a large electrical capacitance which can be constructed on a metal insulating substrate having a small area. Thus, we find Hosen's teaching of using a two-stage stacking structure to provide a large electrical capacitance to a small substrate area to be unrelated to any problem associated with the single multi-layer circuit wiring board of the admitted prior art.

Accordingly, we see no reason, and no persuasive reason has been provided by the examiner, as to why one of ordinary skill in the art would have been motivated or taught to have modified the admitted prior art by moving the power converter and CPU of the admitted prior art to a lower metal plate with the remaining elements on an multi-layer circuit wiring board as advanced by the examiner.

Moreover, even if we made the proposed modifications advanced by the examiner, the limitations of claim 1 would not have been met. Claim 1 recites that the CPU chip is electrically connected to the multi-layer circuit wiring board, between the metal board and the multi-layer circuit wiring board. Claim 1 additionally recites "a control section electrically connected to said multi-layer circuit wiring board, on a surface opposite to the CPU chip provided on said multi-layer circuit wiring board." We find that the language requires that the CPU chip is provided on the multi-layer circuit wiring board. The examiner's proposed modification (answer, page 4) that the CPU and power supply be disposed on the lower metal plate, with the remaining elements on the

upper substrate, is inconsistent with the language of claim 1. The examiner's proposed removal of the CPU chip from the multi-layer circuit wiring board is contrary to the language of claim 1 that the CPU chip is provided on the multi-layer circuit wiring board. Accordingly, we find that the examiner's proposed modification of the prior art would result in a structure that is inconsistent with the limitations of claim 1.

Moreover, even if the proposed modification were made, we find Hosen would only suggest moving the power supply (CPU power converter) to the lower plate. The CPU chip would still remain on the multi-layer circuit wiring board. We find no suggestion that the CPU chip be selected for placement on an opposite side of the multi-layer circuit wiring board. We are cognizant that the admitted prior art teaches that the components can be on both sides of the multi-layer circuit wiring board. However, we would have to resort to speculation to find that the admitted prior art suggests that the CPU chip would be on one side of the multi-layer circuit wiring board and least some of the control elements would be in the other

side of the multi-layer circuit wiring board. Thus, we see no reason to have removed the CPU chip from the multi-layer circuit wiring board it is already on in the admitted prior art, and move it to a location between the lower metal plate and the multi-layer circuit wiring board. With respect to Lin, we find that Lin discloses that the upper substrate can be an multi-layer circuit wiring board, but does not make up for the deficiencies of the admitted prior art and Hosen.

Accordingly, we conclude that the examiner has failed to establish a <u>prima facie</u> case of obviousness of claim 1.

Therefore, the rejection of claim 1, and claims 3-8 and 10, which depend therefrom, is reversed.

We now turn to the rejection of independent claim 2.

Appellants assert (brief, pages 7 and 8) that

Claim 2 differs from claim 1 in that, inter alia, a protection plate is provided at a center portion of the metal board and has a plurality of pillars at side end portions thereof. The subject matter of present claim 2 offers an advantage in terms of protecting the CPU from thermal expansion and contraction of the other components, as described in the specification, e.g., on page 8, lines 18-21.

Appellants further assert (reply brief, pages 1 and 2) that element 1b of Hosen does not meet the limitations of claim 2 with respect to the protection plate because 1b does not have a CPU thereon. Appellants further assert (id.) that element 1c of Hosen does not have pillars called for in claim 2.

The examiner takes the position (answer, page 4) that either insulating layer 1b or upper conductive layer 1c may be considered a protection plate. We disagree. We find that in Hosen (page 1), element 1a is a heat sink made of aluminum. Element 1b of Hosen is an insulating layer formed of epoxy resin. Element 1c is a copper foil conductive pattern. From these teachings of Hosen, we find that the epoxy resin insulating layer does not constitute a plate. Additionally, we find that although the power chip 2 of Hosen is provided on the surface of conductive layer 1c, as are terminals (pillars) 7, we find that copper foil conductive patterns 1c cannot reasonable be construed as a protective plate. We therefore conclude that neither epoxy resin insulating layer 1b nor copper foil conductive pattern 1c meet the claimed protective plate, as advanced by the examiner.

Accordingly, we conclude that the examiner has failed to establish a <u>prima facie</u> case of obviousness of claim 2.

Therefore, the rejection under 35 U.S.C. § 103 of claim 2 and dependent claims 9 and 11-14 is reversed.

We turn next to the rejection of claims 10 and 15 under 35 U.S.C. § 103 as unpatentable over the admitted prior art taken together with Hosen, Lin, and further in view of Karabatsos, we find that Karabatsos shows a cross-shaped pin structure, but does not overcome the deficiencies of the admitted prior art, Hosen and Lin, as discussed, supra.

Accordingly, the rejection of claims 10 and 15 under 35 U.S.C. § 103 is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-15 under 35 U.S.C. § 103 is reversed.

REVERSED

JERRY SMITH)
Administrative Pate	ent Judge)
)
)
)
) BOARD OF PATENT
JOSEPH F. RUGGIERO) APPEALS
Administrative Pate	ent Judge) AND
) INTERFERENCES
)
)
)
STUART S. LEVY)
Administrative Pate	ent Judge	,
AUIIITITACTACTAE PAC	erre o dage	/

JAMES E LEDBETTER
STEVENS DAVIS MILLER & MOSHER LLP
1615 L STREET NW, SUITE 850
P O BOX 34387
WASHINGTON, DC 20043-4387

APPEAL NO. 1999-1454 - JUDGE LEVY APPLICATION NO. 08/596,343

APJ LEVY

APJ RUGGIERO

APJ JERRY SMITH

DECISION: REVERSED

Prepared By:

DRAFT TYPED: 11 Jan 02

FINAL TYPED: